Customer No.: 31561
Application No.: 10/604,821
Docket No.: 11208-US-PA

Amendments To Claims

1. (currently amended) A method of detecting power sources in [~~an integrated circuit (IC)~~] a Dynamic Random Access Memory (DRAM), which comprises:

receiving a first power source, and a second power source; and

discerning whether the first received power source is at a pre-determined power level, and providing a first output signal accordingly to indicate a power level of the first power source, wherein when the first output signal indicates that the first power source is at the pre-determined power level, a power level of the second power source is detected, and a second output signal is provided to indicate a power level of the second power source, a first state of the second output signal indicates a first power level of the second power source, and a second state of the second output signal indicates a second power level of the second power source.

2. (currently amended) A power source detecting circuit for detecting a power source in [~~an integrated circuit (IC)~~] a Dynamic Random Access Memory (DRAM), which comprises:

a first power source detector for detecting whether the [~~IC~~] DRAM operates at a first pre-determined power level, and providing a first output signal to indicate a power level of a first power source;

a second power source detector for detecting whether the [~~IC~~] DRAM operates at a second

pre-determined power level, and providing a second output signal to indicate a power level of [~~the~~] a second power source, wherein a first state of the second output signal allows the [~~IC~~] DRAM to operate at a first data power level, and a second state of the second output signal allows the [~~IC~~] DRAM to operate at a second data power level.

3. (cancelled)

4.(currently amended) The power source detecting circuit of claim 2, wherein the second power source detector provides the first state to indicate the first data power level of the [~~IC~~] DRAM, and provides the second state to indicate the second data power level of the [~~IC~~] DRAM.

5.(currently amended) The power source detecting circuit of claim 2, wherein the first power source detector receives an external power and provides [~~a~~] the first output signal to indicate whether the external power allows the [~~IC~~] DRAM to function normally.

6.(currently amended) The power source detecting circuit of claim 5, wherein the second power source detector receives an external data power and the first output signal, and the second power source detector detects the external data power only when the first output signal indicates that the [~~IC~~] DRAM functions normally.

7.(currently amended) The power source detecting circuit of claim 5, wherein the first output signal of the first power source detector changes state from a high logic state to a low logic state to indicate that the external power source allows the [~~IC~~] DRAM to function normally.

8.(original) The power source detecting circuit of claim 2, wherein the second power source

detector comprises:

a first resistor electrically connecting to an external data power source at one end;

a second resistor electrically connecting to the other end of the first resistor at one end, and electrically connecting to a ground reference at the other end;

a third resistor electrically connecting to the external data power source at one end;

a transistor electrically connecting to a node between the first resistor and the second resistor at a first end, electrically connecting to the ground reference at a second end, and electrically connecting to the other end of the third resistor that is also the output of the second power source detector at a third end.

9. (original) The power source detecting circuit of claim 8, wherein the transistor is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), and the first end is a gate, the second end is a source, and the third end is a drain.

10.(original) The power source detecting circuit of claim 8, wherein the transistor is a bipolar transistor.

11.(original) The circuit in claim 2, wherein the second power source detector comprises:

a P-channel transistor electrically connecting to the external data power at a drain, electrically receiving the output signal of the first power source detector at a gate;

a first resistor electrically connecting to a source of the P-channel transistor at one end;

a second resistor electrically connecting to the other end of the first resister at one end and electrically connecting to a ground reference at the other end;

a first N-channel transistor electrically receiving the output of the first power source detector at a gate, electrically connecting to the ground reference at a source, and electrically connecting to a node between the first resistor and the second resistor at a drain;

a third resistor electrically connecting to the external data power at one end; and

a second N-channel transistor electrically connecting to the node between the first resistor and the second resistor at a gate, electrically connecting to the ground reference at a source, and electrically connecting to the other end of the third resistor at a drain to form the output of the second power source detector.